LODZ UNIVERSITY OF TECHNOLOGY
Faculty of Electrical, Electronic,
Computer and Control Engineering

Doctoral Thesis

ABSTRACT

Design and optimization of photonic systems

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1. Introduction

Nowadays, development of the modern electronic systems becomes more and more difficult due to the limitations of the technology-in-use and ever-increasing demands. One of the general bottlenecks, limiting the speed, the scale and the complexity of electronic systems, is easy, fast and precise signal transmission. The most revolutionary changes was made in the 1970s, when the first optical transmission was introduced. Since then photon began to push the electron out of the interconnect systems due to such features as large bandwidth, low latency, low power requirements, reduced crosstalk, electromagnetic immunity and electrical isolation. Nevertheless, the optical transmission was much cheaper and easier to employ in the long-haul and large bandwidth interconnects. Unfortunately, solutions taken straightforwardly from the telecommunication do not introduce the expected profits in short optical links. That is why new, specially designed optical links must be proposed and optimized instead of the usage of the well-known, but out-of-date solutions designed for the premature cases.

The work is a part of research carried out by the teams from the LEOM lab at Ecole Centrale de Lyon (ECL) and the Department of Semiconductor and Optoelectronics at Lodz University of Technology (DSOD TUL) in the field of photonics systems covering short distance optical transmission lines. It deals with the problem of power budget in optical receivers suitable for short optical transmission lines, used as on-chip and inter-chip connections in Integrated Systems.

The investigation dealt with developing of multi-objective optimization procedure that allows designing such amplifier with minimal power consumption and keeping the magnitude of selected parameters according to assumed conditions. The thesis of the work one can form as follows:

- It is possible to work out the multi-objective optimization procedure allowing design of optical receiver preamplifier for short optical transmission lines characterized by very low power consumption

- The designed preamplifiers are realizable as ASIC structures with the use of available technologies.

2. Optical receiver design

The typical optical receiver circuit is presented in the Fig. 1. The input optical signal is converted into the photocurrent signal by the photodetector (usually p-i-n photodiode) and the following pre-amplifier converts the photocurrent into a low-level voltage signal. Usually, it is followed by a post-amplifier to meet the amplification and bandwidth requirements as well as to convert small voltage signals into rail-to-rail voltage, e.g. in digital applications. The output logic block produces a regenerated logic signal that is often re-timed with a clock extracted from the data stream.

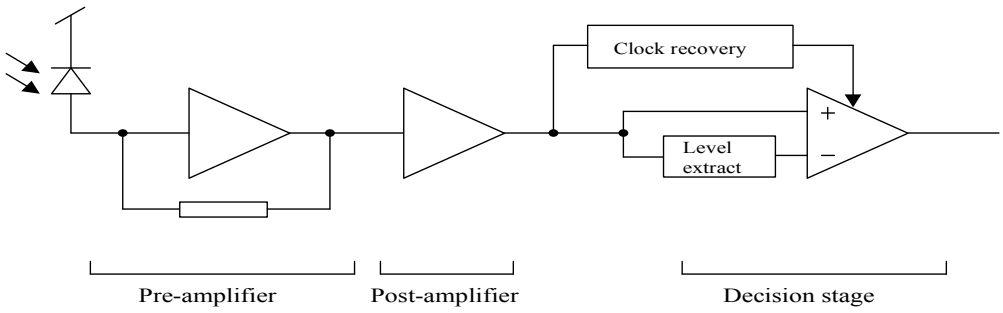

Fig. 1 Circuit of the optical receiver.

This work is focused on the first two elements: photodiode and preamplifier, with all the optimization mechanism applied to investigate the preamplifier circuit in the concept of transimpedance amplifier (TIA). The parameters of TIA determine the quality of the entire interconnect parameters and its optimization is difficult due to some contradictory requirements like low power dissipation, large bandwidth, high transimpedance gain.

3. Multi-objective optimization

In the proposed multi-objective optimization solution the Pareto frontier method was applied together with custom-made implementation of the genetic algorithm. This optimization tool was implemented in Java programming language, creating a software called RUNE (acronym from the phrase *platfoRm aUtomated aNy dEsign*). The program uses also Spectre simulation engine (available in Cadence package) as an external tool for getting DC and AC analysis of each tested solution. Fig. 2a-f shows an example of the RUNE optimization process results, captured after few subsequent loops. Two main phenomena are recorded, confirming the successful optimization: i) total number of Pareto frontiers is decreasing, finally equal to 1

(stoppage criteria of the entire optimization process), and ii) all the points move towards the hyperbola-shape, showing the best (minimum in this case) available level of performances.

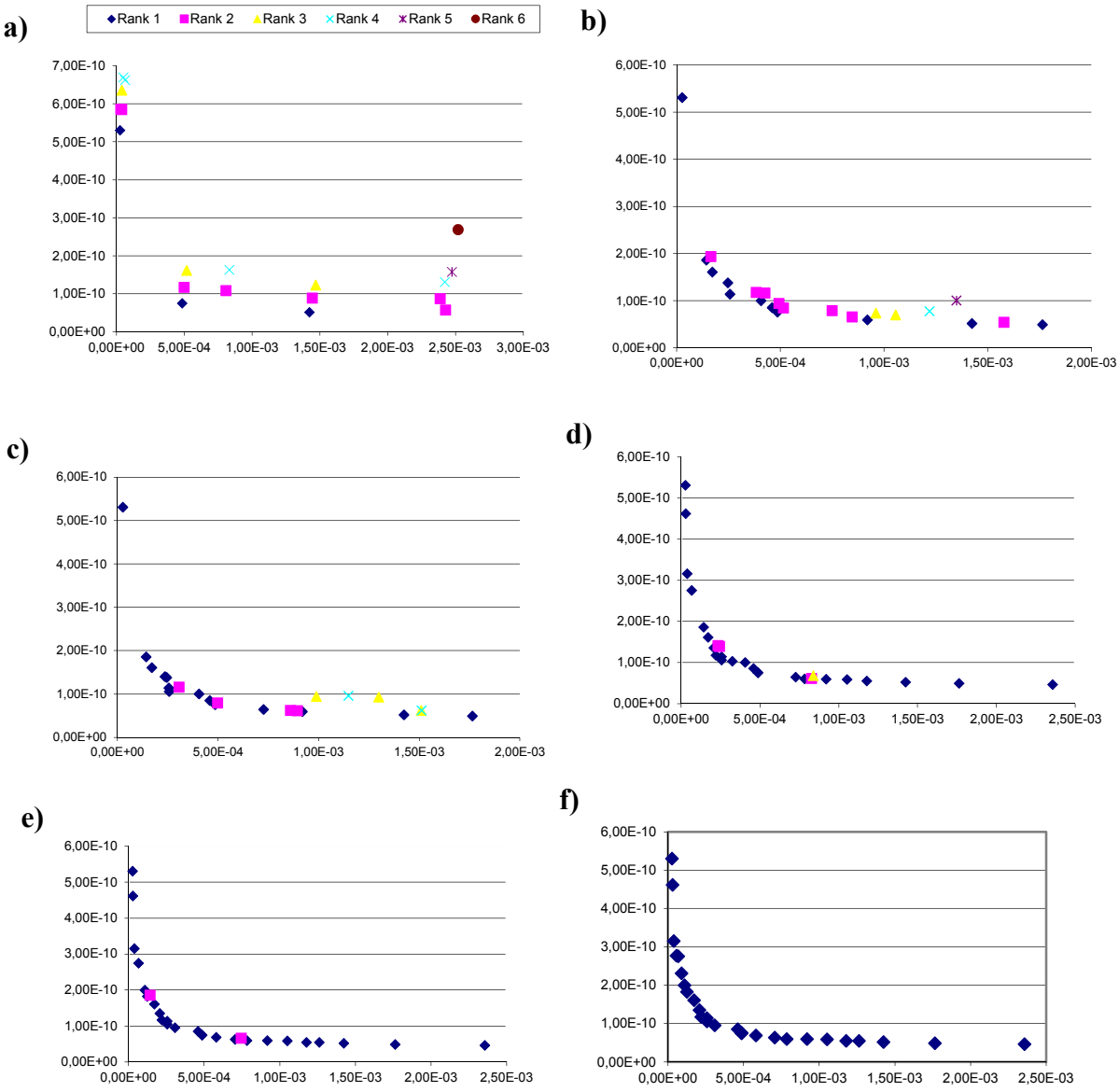

Fig. 2. Pareto frontiers division obtained in subsequent optimization loop (X axis: dissipated power [W], Y-axis: 1/circuit bandwidth [Hz^{-1}])

Together with the introduced optimization procedure, a figure of merit was also proposed as a criteria for comparison of the solutions equal in the Pareto sense. This coefficient was used inside of the optimization process and also for selecting the best candidate to ASIC realization.

The TIA circuits were chosen in two technologies: CMOS and Si/SiGe HBT, as both have the potential to be functional in the on-chip applications. Among the circuit topologies,

selected on the base of published circuits review, five most promising were selected and optimized with the use of RUNE. Eventually, two of the most promising circuits were selected for the practical realization as ASIC: 1-stage HBT and 3-stage HBT. For them all the required layout and post-layout analysis were done, giving the final set of masks for the foundry.

4. ASIC realization and measurements

The physical realization of the structures was done by the IHP company, located in Germany in Frankfurt (Oder) and delivered in 3 forms: open (plain) structures and packaged into two different cases, DIL24 and SOIC24. All of them were tested with the use of the measurement setup built in the laboratory at DSOD, TUL. In the Fig. 3 the ASIC structure in both packages is presented.

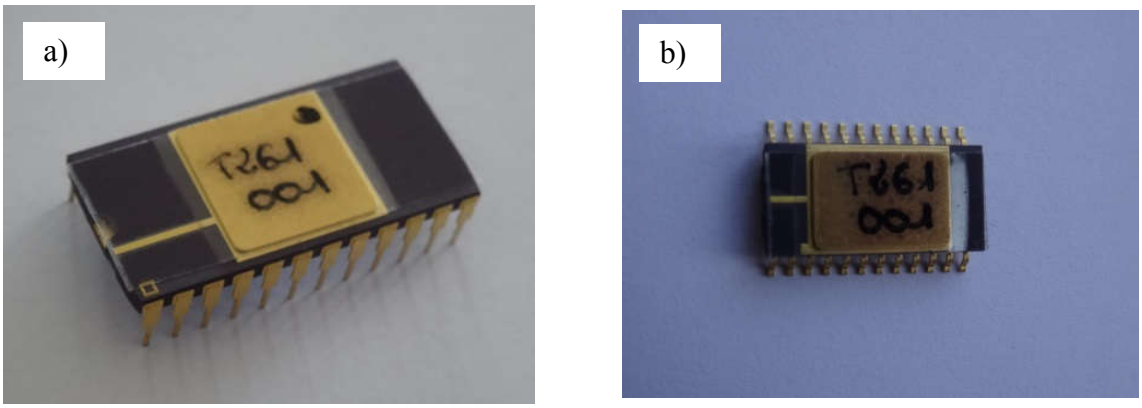

Fig. 3. ASIC in both packages: a) DIL24, b) SOIC24.

Unfortunately, the 3-stage HBT circuits had an error in manufacturing – a layer of polysilicon was missed on the resistor pins and for this reason all the results refer to 1-stage HBT TIA. Nevertheless, the DC measurement of the 1-stage HBT receiver in the DIL24 package confirmed in/out values driven from the Spectre simulation.

AC measurements of the receiver give diverse results, depending on the package, with the remark, that better values are reached for SOIC24, confirming that this is more suitable package for high frequency signals. Table 1 contains the best measured bandwidth and transimpedance gain and Fig. 4 shows the AC characteristics for both package types.

Table 1

The best results gained in the AC measurements.

Package	Voltage supply	Bandwidth	Transimpedance gain
DIL24	1.3V	0.6 GHz	0.4 kΩ
SOIC24	2.1V	1.2 GHz	0.7 kΩ

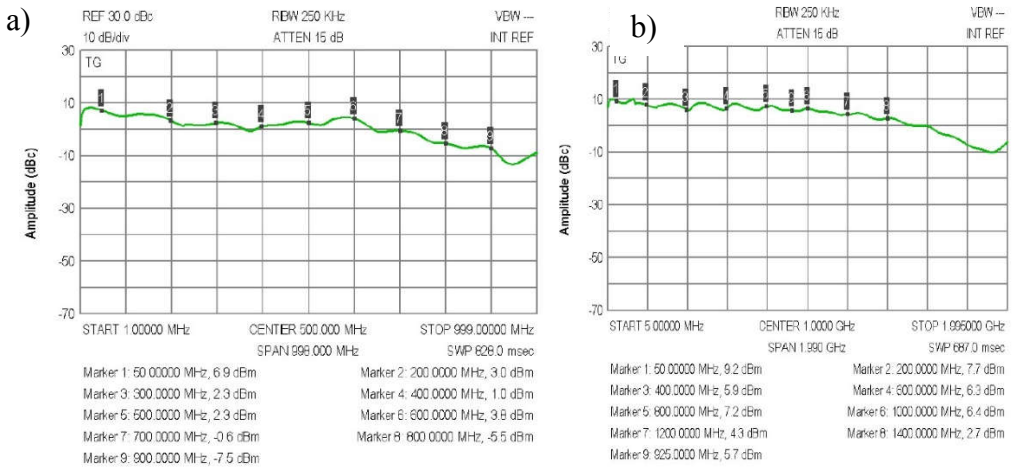

Fig. 4. The best results of the AC analysis of the 1-st HBT receiver: a) DIL24 package, b) SOIC24 package.

5. Summary

On the base of the presented results one can conclude that the thesis has been proved. It is possible to develop the optimization procedure searching for the optical receiver preamplifier for short optical transmission lines characterized by very low power consumption and other constraints. Also, the designed preamplifiers are realizable as ASIC structures with the use of available technologies.

The results obtained in this work allow also for the conclusion, that heterojunction bipolar technology Si/SiGe is indeed an interesting and promising alternative for CMOS also III-V compounds, especially in optoelectronics. Not only it is relatively cheap and can be compatible with CMOS, but also it has a large application field in the high frequency circuits and integrated optoelectronics.